local register sets are partitioned from a register file." Office Action mailed November 23, 2001, p. 2, ll. 7-8.

Nishimoto is apparently cited for the teaching of VLIW. Office Action mailed May 1, 2002, p. 3.

Luan discloses a plurality of memories 104 which may be shared by a CPU and a plurality of peripheral devices using a plurality of memory configuration controllers 202 corresponding to the memories 104. (See Luan, Figure 2.) The Examiner cites Luan for the teaching of "programmably configurable." Office Action mailed May 1, 2002, p. 4, line 1.

However, the Examiner provides no specific cite to a portion of Luan regarding such teaching as required by MPEP §§ 706.02(j) other than a general reference to the Abstract and Summary. The applicants respectfully submit that the particular parts of the cited references that the Examiner has relied upon have not been designated as nearly as practicable, and the pertinence of each reference has not been clearly explained, both as required by 37 C.F.R. § 1.104(c)(2). Applicants respectfully request that the Examiner more specifically point out portions of Luan upon which the Examiner believes elements of the claims read. Nevertheless, the applicants have made every effort to respond to the rejections outlined by the Examiner.

Section 103(a) Rejection of Claims 1-14 and 23-28 (primarily in view of Yung and Luan)

Independent claims 1 and 23 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yung in view of Luan. Yung discloses a processor with multiple threads. Luan discloses memories coupled between a CPU and peripheral devices, each memory being coupled through one of a plurality of memory configuration controllers.

Applicants respectfully assert that there is not a proper basis for a combination of Yung and Luan in this fashion. First, there is no suggestion within either of these references that would lead one to the other of the references. For example, there is no suggestion within Yung of a potential benefit of using memory configuration controllers such as those of Luan, and there is no suggestion within Luan as to how the memory configuration controllers could be advantageously implemented to configure a local register buffer as well as the global register file within the processor of Yung. The Examiner appears to have used the teaching of the present

application in an attempt to construct the invention with the advantage of the hindsight provided by the present application. "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure." MPEP 706.02(j); In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991). Thus, a *prima facie* case of unpatentability has not been made, and independent claims 1 and 23 are allowable over Yung and Luan for at least this reason.

Even if Yung and Luan are properly combinable in this context, Yung and Luan do not disclose, alone or in combination, a processor including "a register file that is divided into a plurality of register file segments" which are further "partitioned into global registers and local registers," much less such a processor in which the "global registers and the...local registers are programmably configurable," all as required by independent claim 1.

For example, although Yung discloses a global register file/memory 290 separate from execution units 241 and a number of local register buffers 241d in each execution unit 241, Yung and Luan do not disclose, alone or in combination, "a *register file* that is divided into a plurality of *register file segments*...partitioned into *global registers* and *local registers*," all as required by independent claim 1 (emphasis added). The highlighted hierarchy is not taught. Further, the Examiner has stated that "Yung does not disclose whether the global register and the local register sets [of Yung] are partitioned from a register file." (Office Action mailed November 23, 2001, p. 2, ll. 7-8.) In the cited Office Action, the Examiner cited Jenson for the partition teaching. In the present Office Action responsive to Applicant's arguments filed August 18, 2001, the Examiner has withdrawn the rejection in view of Jenson's alleged partitioning, but has not cited any additional reference for the partition teaching (citing Luan only for the teaching of a programmably configurable memory). For at least this reason, a *prima facie* case of unpatentability has not been made regarding independent claim 1. Therefore, independent claim 1 is allowable over Yung and Luan for at least this reason.

Also, although Figure 2 of Luan discloses a plurality of memories 104 which may be shared using a plurality of corresponding memory configuration controllers 202, Yung and Luan do not disclose, alone or in combination, a processor including "a register file that is divided into a plurality of register file segments...partitioned into global registers and local registers," much

less such a processor in which the "*global registers and the...local registers are programmably configurable*," all as required by independent claim 1 (emphasis added). Yung's local register buffers 241d are resident within each respective execution unit 241, and are not accessible to other execution units. It is unclear how the addition of Luan's memory configuration controllers to Yung's execution units would be at all beneficial to Yung. Therefore, independent claim 1 is allowable over Yung and Luan for at least this reason.

Regarding independent claim 23, Yung and Luan do not disclose, alone or in combination, a method of operating a processor including "a register file divided into a plurality of register file segments" and "partitioning the register file segments into global registers and local registers," much less such a method including "programmably partitioning the register file so that the number of global registers and the number of the local registers are selectable and variable," all as required by independent claim 23.

For example, although Yung discloses a global register file/memory 290 separate from execution units 241 and a number of local register buffers 241d in each execution unit 241, Yung and Luan do not disclose, alone or in combination, "a *register file* divided into a plurality of *register file segments*" much less "partitioning the *register file segments* into *global registers* and *local registers*," all as required by independent claim 23 (emphasis added). The Examiner has stated that "Yung does not disclose whether the global register and the local register sets [of Yung] are partitioned from a register file." (Office Action mailed November 23, 2001, p. 2, ll. 7-8.) In the cited Office Action, the Examiner cited Jenson for the partition teaching. In the present Office Action responsive to Applicant's arguments filed August 18, 2001, the Examiner has withdrawn the rejection in view of Jenson's alleged partitioning, but has not cited any additional reference for the partition teaching (citing Luan only for the teaching of a programmably configurable memory). For at least this reason, a *prima facie* case of unpatentability has not been made regarding independent claim 23. Therefore, independent claim 23 is allowable over Yung and Luan for at least this reason.

Also, although Figure 2 of Luan discloses a plurality of memories 104 which may be shared using a plurality of corresponding memory configuration controllers 202, Yung and Luan do not disclose, alone or in combination, a method of operating a processor including "a register

file divided into a plurality of register file segments" which in turn are partitioned "into global registers and local registers," much less such a method including "programmably partitioning the register file so that the number of global registers and the number of the local registers are selectable and variable," all as required by independent claim 23. Yung's local register buffers 241d are resident within each respective execution unit 241, and are not accessible to other execution units. It is unclear how the addition of Luan's memory configuration controllers to Yung's execution units would be at all beneficial to Yung. Therefore, independent claim 23 is allowable over Yung and Luan for at least this reason.

Thus, Applicants respectfully submit that each of the independent claims 1 and 23 clearly distinguish from the cited references for at least the reasons recited above. Each of the claims dependent from independent claims 1 and 23 distinguishes from the cited art for at least the same reasons as the independent claim from which it depends. Accordingly, Applicants respectfully submits that claims 1-14 and 23-28 are also allowable over Yung and Luan.

Section 103(a) Rejection of Claims 15-22 in view of Yung, Luan and Nishimoto

Independent claim 15 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Yung in view of Luan (cited for the teaching of "programmably configurable") and further in view of Nishimoto (cited for the teaching of VLIW). Applicants renew the objection to the combination of Yung with Luan, and further with Nishimoto as set forth above.

Even if Yung, Luan and Nishimoto are combinable, Yung, Luan and Nishimoto do not disclose, alone or in combination, a processor including "a register file...divided into a plurality of register file segments...including a plurality of registers that are partitioned into global registers and local registers," all as required by independent claim 15. For example, although Yung discloses a global register file/memory 290 separate from execution units 241 and a number of local register buffers 241d in each execution unit 241, Yung and Luan do not disclose, alone or in combination, "a *register file*...divided into a plurality of *register file segments*...including a plurality of registers that are partitioned into *global registers* and *local registers*," all as required by independent claim 15 (emphasis added). The Examiner has stated that "Yung does not disclose whether the global register and the local register sets [of Yung] are partitioned from a register file." (Office Action mailed November 23, 2001, p. 2, ll. 7-8.) In the

cited Office Action, the Examiner cited Jenson for the partition teaching. In the present Office Action responsive to Applicant's arguments filed August 18, 2001, the Examiner has withdrawn the rejection in view of Jenson's alleged partitioning, but has not cited any additional reference for the partition teaching (citing Luan only for the teaching of a programmably configurable memory). For at least this reason, a *prima facie* case of unpatentability has not been made regarding independent claim 15.

Therefore, independent claim 15 is allowable over Yung and Luan for at least the above reasons. Each of claims 16-22 dependent from independent claim 15 distinguishes from the cited art for at least the same reasons as independent claim 15. Accordingly, Applicants respectfully submits that claims 16-22 are also allowable over Yung and Luan.

Conclusion

Claims 1-28 remain pending in the application. The rejection of claims 1-28 under 35 U.S.C. 103(a) as being unpatentable over Yung in view of Luan, and sometimes further in view of Nishimoto has been traversed.

In view of the amendments and remarks set forth herein, the application and claims therein are believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be amenable to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to Commissioner for Patents, Washington, D.C. 20231 on the date shown below.

Michael P. Noonan — July 31, 2002 (Date)

Respectfully submitted,

Michael P. Noonan, Reg. No. 42,038
Attorney for Applicant(s)
(512) 347-9030
(512) 347-9031 (fax)